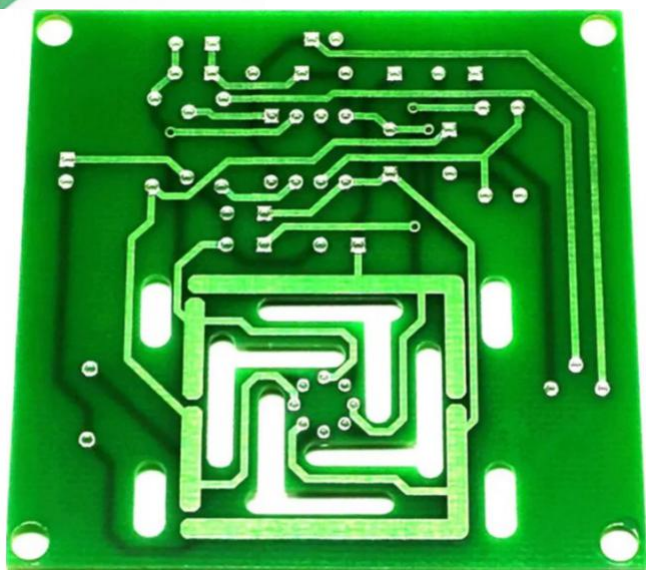
*Bahan Ajar*

**Modul Praktikum**

# DESAIN DAN SIMULASI RANGKAIAN ELEKTRONIKA

Kode Matakuliah: SKO21425



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**2023**

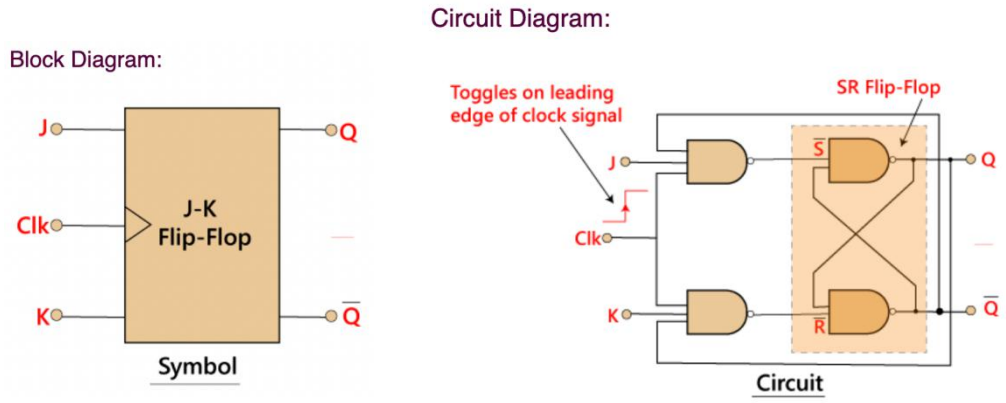
# Modul 6

## JK Flip Flop

1. JK flip flop

The JK flip flop is one of the most used flip flops in digital circuits. The JK flip flop is a universal flip flop having two inputs 'J' and 'K'. In SR flip flop, the 'S' and 'R' are the shortened abbreviated letters for Set and Reset, but J and K are not. The J and K are themselves autonomous letters which are chosen to distinguish the flip flop design from other types. The JK flip flop work in the same way as the SR flip flop work. The JK flip flop has 'J' and 'K' flip flop instead of 'S' and 'R'. The only difference between JK flip flop and SR flip flop is that when both inputs of SR flip flop is set to 1, the circuit produces the invalid states as outputs, but in case of JK flip flop, there are no invalid states even if both 'J' and 'K' flip flops are set to 1.

The JK Flip Flop is a gated SR flip-flop having the addition of a clock input circuitry. The invalid or illegal output condition occurs when both of the inputs are set to 1 and are prevented by the addition of a clock input circuit. So, the JK flip-flop has four possible input combinations, i.e., 1, 0, "no change" and "toggle". The symbol of JK flip flop is the same as SR Bistable Latch except for the addition of a clock input.




In SR flip flop, both the inputs 'S' and 'R' are replaced by two inputs J and K. It means the J and K input equates to S and R, respectively. The two 2-input AND gates are replaced by two 3-input NAND gates. The third input of each gate is connected to the outputs at Q and Q'. The cross-coupling of the SR flip-flop permits

the previous invalid condition of (S = "1", R = "1") to be used to produce the "toggle action" as the two inputs are now interlocked.

If the circuit is "set", the J input is interrupted from the "0" position of Q' through the lower NAND gate. If the circuit is "RESET", K input is interrupted from 0 positions of Q through the upper NAND gate. Since Q and Q' are always different, we can use them to control the input. When both inputs 'J' and 'K' are set to 1, the JK toggles the flip flop as per the given truth table.

The JK flip flop is an improved clocked SR flip flop. But it still suffers from the "race" problem. This problem occurs when the state of the output Q is changed before the clock input's timing pulse has time to go "Off". We have to keep short timing plus period (T) for avoiding this period

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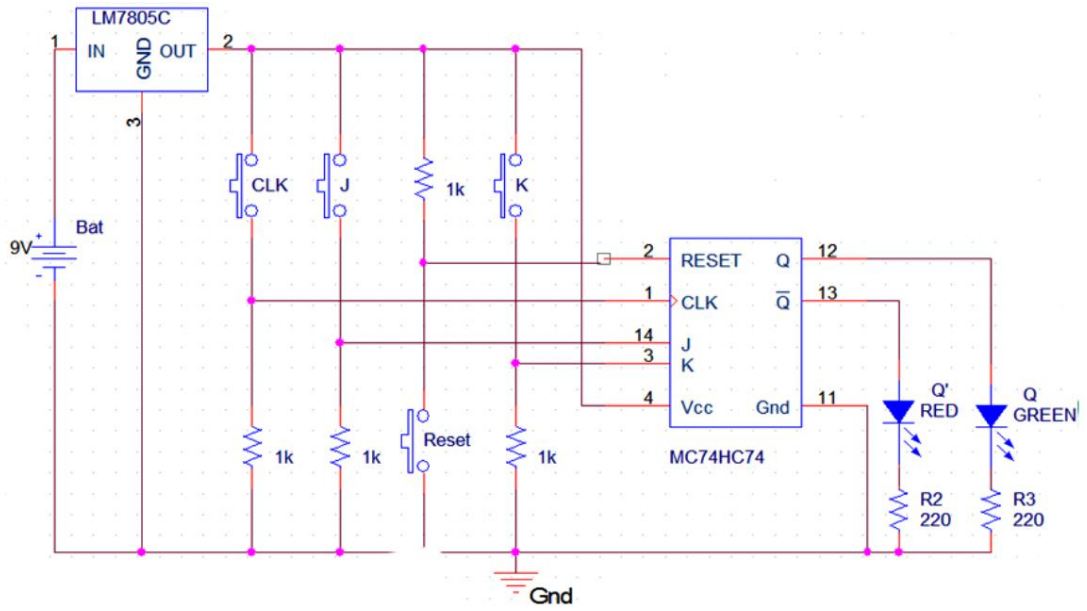
## JOBSHEET 6

Lakukan Simulasi JK Flip Flop menggunakan software simulator seperti pada gambar skema di bawah ini dan jelaskan tahapan perakitan dan hasil simulasinya.

JK FLIP FLOP CIRCUIT USING 74LS73



LAPORAN HASIL PERCOBAAN: