Bahan Ajar

Modul Praktikum

DESAIN DAN SIMULASI RANGKAIAN ELEKTRONIKA

Kode Matakuliah: SKO21425

Penyusun:

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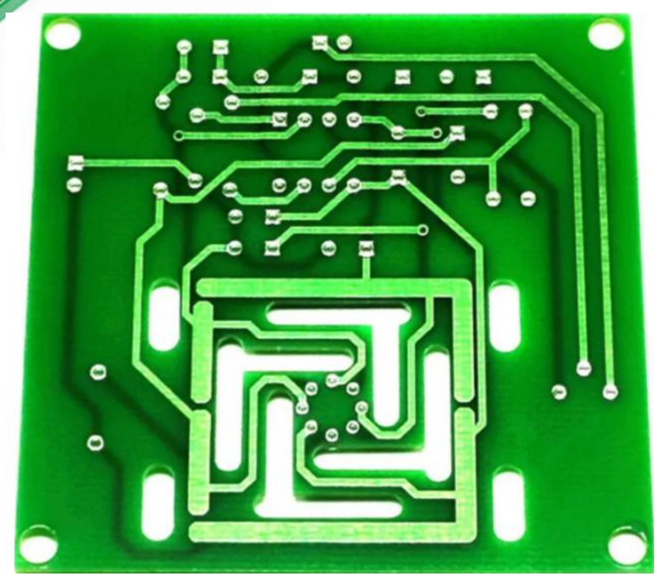

PROGRAM STUDI SISTEM KOMPUTER

FAKULTAS ILMU KOMPUTER

INSTITUT INFORMATIKA DAN BISNIS DARMAJAYA

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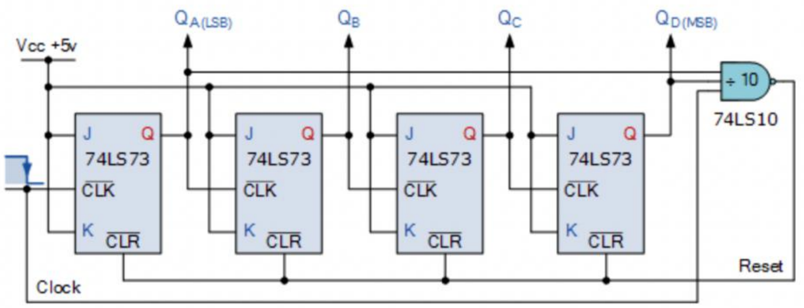
Modul 10

Asynchronous Counter

1. Asynchronous Counters

Asynchronous Counters use flip-flops which are serially connected together so that the input clock pulse appears to ripple through the counter. An Asynchronous counter can have 2n-1 possible counting states e.g. MOD-16 for a 4-bit counter, (0-15) making it ideal for use in Frequency Division applications. But it is also possible to use the basic asynchronous counter configuration to construct special counters with counting states less than their maximum output number. For example, modulo or MOD counters. This is achieved by forcing the counter to reset itself to zero at a pre-determined value producing a type of asynchronous counter that has truncated sequences. Then an n-bit counter that counts up to its maximum modulus (2n) is called a full sequence counter and a n-bit counter whose modulus is less than the maximum possible is called a truncated counter. But why would we want to create an asynchronous truncated counter that is not a MOD-4, MOD-8, or some other modulus that is equal to the power of two. The answer is that we can by using combinational logic to take advantage of the asynchronous inputs on the flip-flop. If we take the modulo-16 asynchronous counter and modified it with additional logic gates it can be made to give a decade (divide-by-10) counter output for use in standard decimal counting and arithmetic circuits. Such counters are generally referred to as Decade Counters. A decade counter requires resetting to zero when the output count reaches the decimal value of 10, ie. when DCBA = 1010 and to do this we need to feed this condition back to the reset input. A counter with a count sequence from binary “0000” (BCD = “0”) through to “1001” (BCD = “9”) is generally referred to as a BCD binary-coded-decimal counter because its ten state sequence is that of a BCD code but binary decade counters are more common.

Asynchronous Decade Counter



This type of asynchronous counter counts upwards on each trailing edge of the input clock signal starting from 0000 until it reaches an output 1001 (decimal 9). Both outputs QA and QD are now equal to logic “1”. On the application of the next clock pulse, the output from the 74LS10 NAND gate changes state from logic “1” to a logic “0” level. As the output of the NAND gate is connected to the CLEAR (CLR) inputs of all the 74LS73 J-K Flip-flops, this signal causes all of the Q outputs to be reset back to binary 0000 on the count of 10. As outputs QA and QD are now both equal to logic “0” as the flip-flop’s have just been reset, the output of the NAND gate returns back to a logic level “1” and the counter restarts again from 0000. We now have a decade or Modulo-10 up-counter.

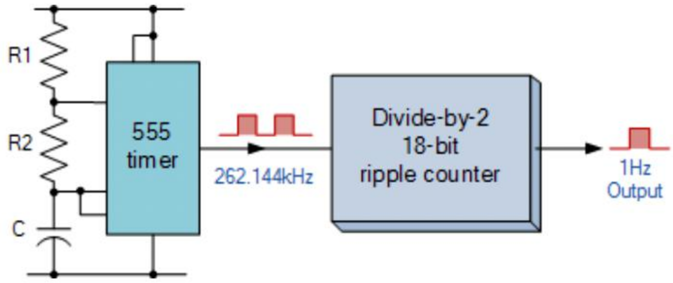
Decade Counter Truth Table

Clock Count	Output bit Pattern				Decimal Value
	QD	QC	QB	QA	
1	0	0	0	0	0
2	0	0	0	1	1
3	0	0	1	0	2
4	0	0	1	1	3
5	0	1	0	0	4
6	0	1	0	1	5
7	0	1	1	0	6
8	0	1	1	1	7
9	1	0	0	0	8
10	1	0	0	1	9
11	Counter Resets its Outputs back to Zero				

2. 1Hz timing signal from a 18-bit asynchronous ripple counter

This is of course a very simplistic example of how to produce accurate timing frequencies, but by using high frequency crystal oscillators and multi-bit frequency dividers, precision frequency generators can be produced for a full range of applications ranging from clocks or watches to event timing and even electronic piano/synthesizer or music type applications.

1Hz timing signal from a 18-bit asynchronous ripple counter



In asynchronous circuits this delay is called the Propagation Delay giving the asynchronous ripple counter the nickname of "propagation counter" and in some high frequency cases this delay can produce false output counts.

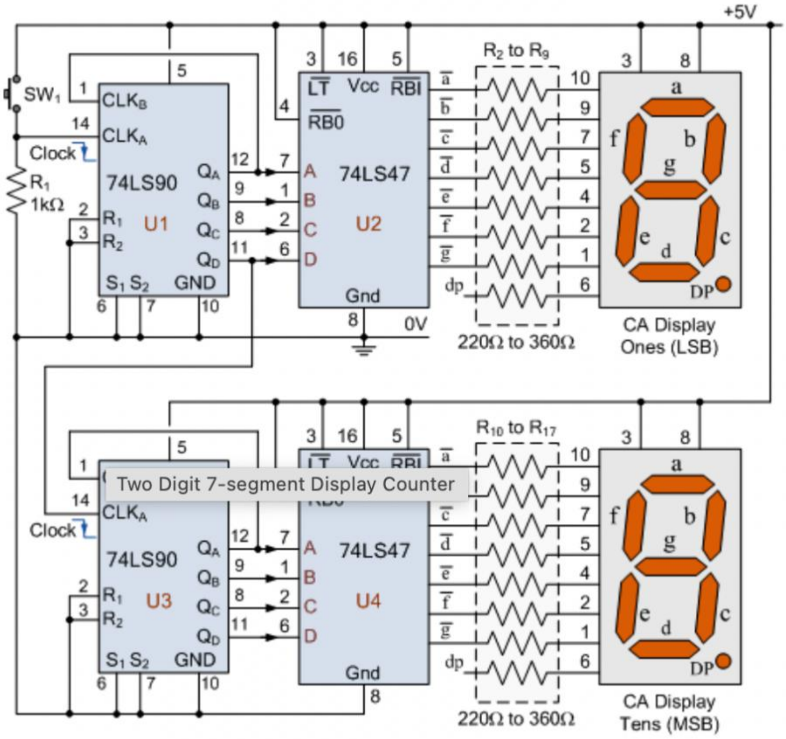
In large bit ripple counter circuits, if the delay of the separate stages are all added together to give a summed delay at the end of the counter chain the difference in time between the input signal and the counted output signal can be very large. This is why the Asynchronous Counter is generally not used in high frequency counting circuits were large numbers of bits are involved.

Also, the outputs from the counter do not have a fixed time relationship with each other and do not occur at the same instant in time due to their clocking sequence. In other words the output frequencies become available one by one, a sort of domino effect. Then, the more flip-flops that are added to an asynchronous counter chain the lower the maximum operating frequency becomes to ensure accurate counting. To overcome the problem of propagation delay Synchronous Counters were developed.

JOBSHEET 10

Lakukan Simulasi Asynchronous Counters menggunakan software simulator dengan IC 74HC161 (4 bit synchronous BCD Counter with Asynchronous reset dan jelaskan tahapan perakitan dan hasil simulasinya.

Two Digit 7-segment Display Counter



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