

Bahan Ajar

Chapter 12



Materi Pembelajaran

Matakuliah :

# DESAIN DAN SIMULASI RANGKAIAN ELEKTRONIKA

Kode Matakuliah : SKO 21425

Prodi : **SISTEM KOMPUTER**

Dosen Pengampu Matakuliah:

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## Synchronous binary counter

A synchronous counter, in contrast to an asynchronous counter, is one whose output bits change state simultaneously, with no ripple.

The only way we can build such a counter circuit from J-K flip-flops is to connect all the clock inputs together, so that each and every flip-flop receives the exact same clock pulse at the exact same time.

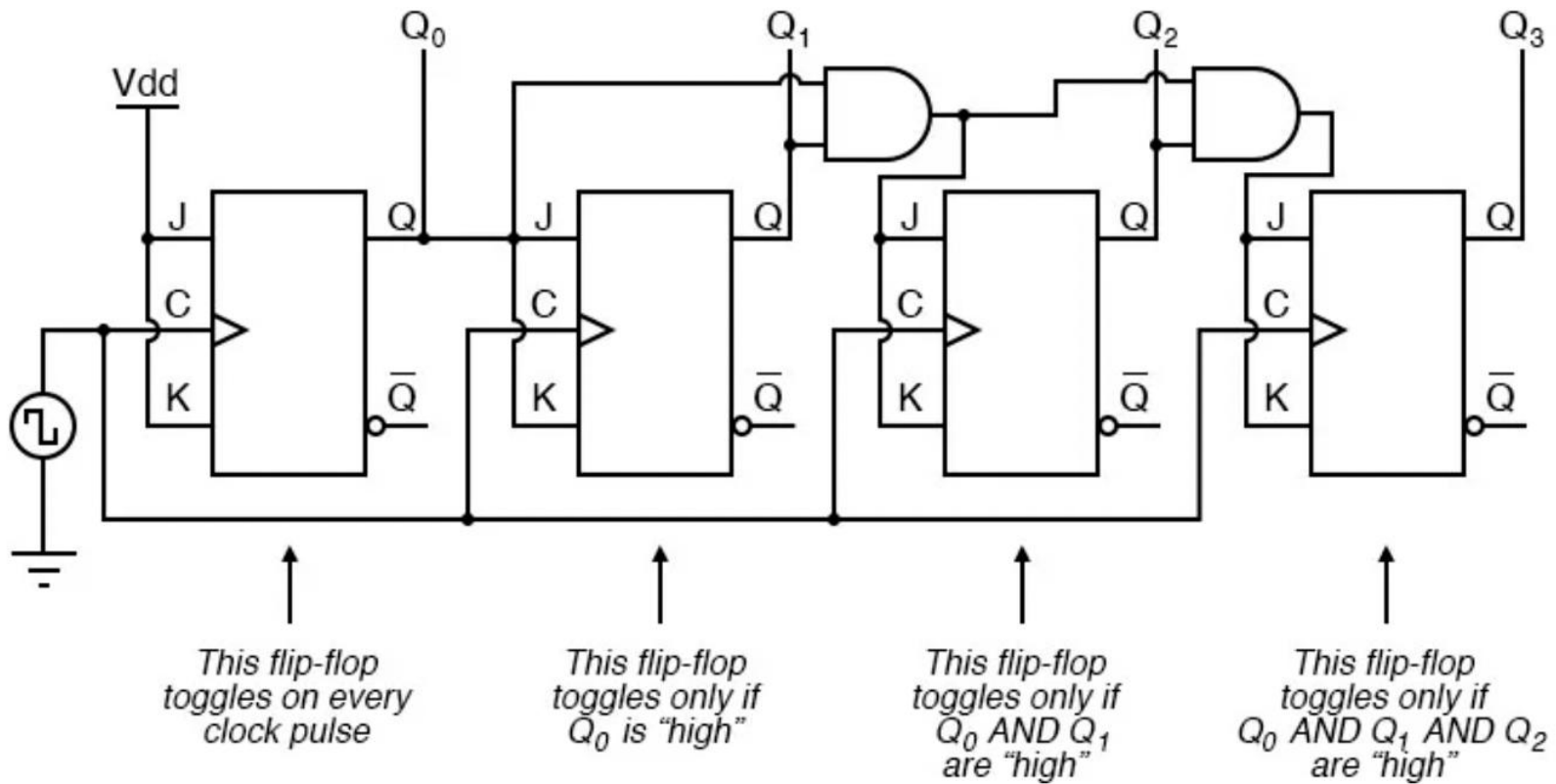
## Synchronous UP counter

If we enable each J-K flip-flop to toggle based on whether or not all preceding flip-flop outputs (Q) are “high,” we can obtain the same counting sequence as the asynchronous circuit without the ripple effect, since each flip-flop in this circuit will be clocked at exactly the same time:



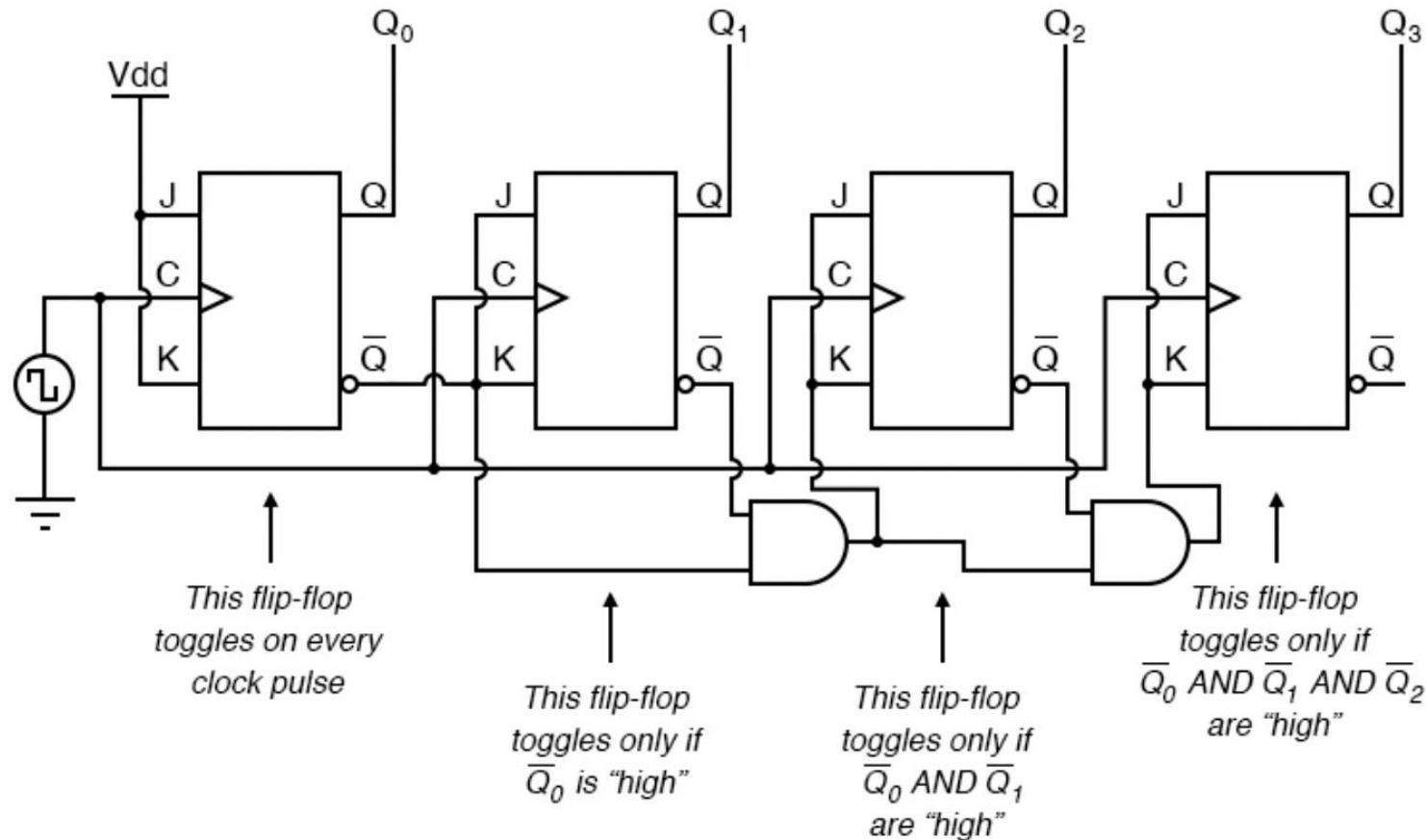
# Synchronous UP counter

A four-bit synchronous "up" counter



# Synchronous Down counter

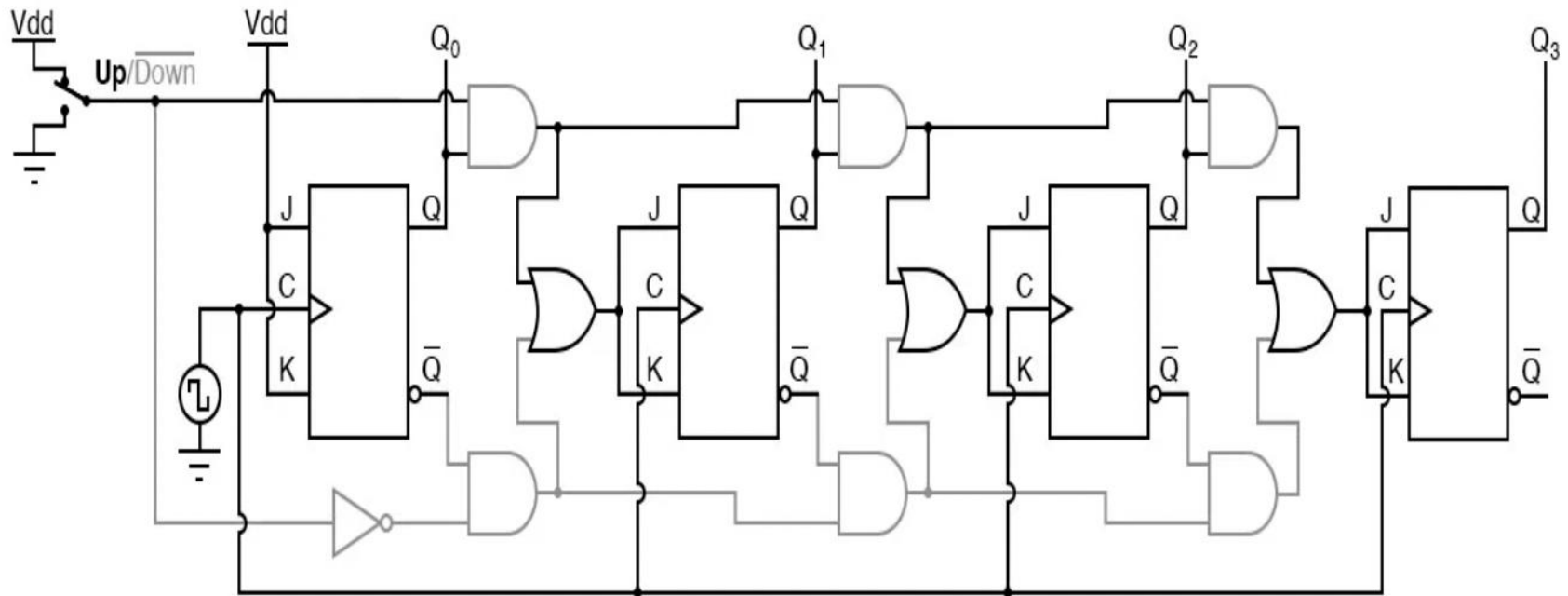
A four-bit synchronous "down" counter



## Chapter 12

# Counter Circuit with Selectable “up” and “down” Count Modes

Counter in “up” counting mode





Tugas Mandiri (teori):

Lakukan pembuatan skema rangkaian Synchronous Up dan Down Counter 7 Segment menggunakan software simulator

Tugas Mandiri (prakt):

Lakukan Simulasi Synchronous Up dan Down Counter 7 Segment menggunakan software simulator dan jelaskan hasil simulasinya.

**end**

